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10/527,098	03/09/2005	Rob Anne Beuker	NL02 0815 US	3804

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DLA PIPER LLP (US)
2000 UNIVERSITY AVENUE
EAST PALO ALTO, CA 94303

EXAMINER	
MA, TIZE	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/527,098	BEUKER, ROB ANNE	
	Examiner	Art Unit	
	TIZE MA	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7 and 9-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,3-4,7,9-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/4/2010 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 2, 4, 5, 7, 9, 10, and 14-21 have been considered but are moot in view of the new ground(s) of rejection. Independent claims 1-2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US. 5,587,962), and in view of Badger (US. 5,973,664), and further in view of Bloxham et al (U.S. 6,904,473 B1).

3. Regarding independent claim 1, the added feature by the amendment is a common way for reading a consecutive block of data from a memory. Although the references of Hashimoto et al and Badger do not explicitly disclose the feature, the feature would be inherent. Bloxham et al is introduced as a supporting document to show the feature, see column 4, lines 34-53. The combination of Hashimoto et al, Badger, and Bloxham et al renders the claim 1 obvious to one of ordinary skill in the art at the time of the invention. Therefore claim 1 remains rejected. The same rationale applies to claims 2 and 9, and the dependent claims.

4. In addition, the features added to claims 11, 14, 16, and 19 by the amendment are also the standard way to read or transfer a pixel block line by line, or block by block (e.g., see Badger, column 8, lines 16-33). Therefore these claims remain rejected. The same rationale applies to claims 12-13, 15, 17-18, and 20-21.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 7 and 10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 7 and 10 recite a "computer readable medium". However, the specification is silent about the medium. The broadest reasonable interpretation of the claims covers a signal per se, which is non-statutory subject matter. It is suggested that a claim drawn to such a computer readable medium that covers both transitory and non-transitory embodiments may be amended to narrow the claim to cover only statutory embodiments to avoid a rejection under 35 U.S.C. § 101 by adding the limitation "non-transitory" to the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 4-5, 7, 9-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US. 5,587,962), and in view of Badger (US. 5,973,664), and further in view of Bloxham et al (U.S. 6,904,473 B1).

9. Regarding claim 1, Hashimoto et al teaches a method of operating a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) , wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer (address sequencers 40a and 40b in Fig. 2), each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line (address generators 28a and 28b in Fig. 2) , the method comprising:

storing a full table of line pointers for different sequences of video data to be displayed in the memory (column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost) ; and

operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from line pointers in address table register means with the output of a pixel counter, and in a second mode wherein line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means (Fig. 3 and column 4, lines 8-11. Two modes of operations, the random access mode and the serial mode. The random access mode is equivalent to the first mode in the instant claim, and the serial mode is equivalent to the second mode).

10. However, Hashimoto et al does not teach a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder. In addition, although Hashimoto et al does not explicitly teach wherein operating the driving circuit in the second mode includes: setting a base address of the block of line pointers to zero; reading a line pointer that corresponds to the base address of zero from the memory into the address table register means; and successively increasing the base address by one and reading the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means, this is a standard way of sequentially reading a block of data stored consecutively in the memory.

11. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence, is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address.

Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

12. Bloxham et al, also in the same field of endeavor, show the way of sequentially reading a block of data stored consecutively in the memory (column 4, lines 34-53).

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method as shown in Hashimoto et al by using a block of line pointers and forming the memory address from line counter and pixel counter as shown in Badger for organizing the display data in the memory in an intuitive manner, and using the common way of sequentially reading a block of data stored consecutively in the memory as shown in Bloxham et al.

14. Regarding claim 2, Hashimoto et al teaches a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) comprising :

a memory for video data to be displayed (memory 24 in Fig. 2) and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for line pointers from said table of line pointers (address sequencers 40a and 40b in Fig. 2); and

means for successively updating the address table register means with subsequent line pointers from the full table of line pointers that is contained in the memory (column

4, lines 8-18, Serial access mode; column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost.)

a pixel counter (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As seen in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.), the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (Fig. 3 and column 4, lines 8-11. The random access mode); and

switching means, by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers from the full table of line pointers that is contained in the memory (column 4, lines 8-18. Serial access mode and random access mode).

15. However, Hashimoto et al does not teach address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder. In addition, although Hashimoto et al does not explicitly teach wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the

corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means, this is a standard way of sequentially reading a block of data stored consecutively in the memory.

16. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence, is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address. Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

17. Bloxham et al, also in the same field of endeavor, show the way of sequentially reading a block of data stored consecutively in the memory (column 4, lines 34-53).

18. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device as shown in Hashimoto et al by using address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means

using an adder for organizing the display data in the memory in an intuitive manner, as shown in Badger, and using the common way of sequentially reading a block of data stored consecutively in the memory as shown in Bloxham et al.

19. Regarding claim 4, Hashimoto et al teaches that the memory comprises a full table of line pointers for different sequences of video data to be displayed (column 5, lines 50-52. Writing addresses generated by the address generator into memory).

20. Claim 5 is rejected based on the same reason as to claim 2 since the driving circuit for display system is always connected to a display system if it is operational.

21. Claim 7 is rejected based on the same reason as to claim 2 since they are the software implementation which is necessary to make the circuit in claim 2 operational.

22. Regarding claim 9, Hashimoto et al teaches a driving circuit for a display system comprising:

a memory (Fig. 2, 24) for video data to be displayed and coupled thereto an address sequence for controlling the sequence of writing and/or reading the video data in said memory (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2.)

means for successively updating the address table register means with subsequent line pointers from the full table of line pointers that is contained in the memory (column 4, lines 8-18, serial access mode; column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost); and

a pixel counter, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As seen

in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.)

23. However, Hashimoto et al does not teach address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder. In addition, although Hashimoto et al does not explicitly teach wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means, this is a standard way of sequentially reading a block of data stored consecutively in the memory.

24. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence,

is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address. Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

25. Bloxham et al, also in the same field of endeavor, show the way of sequentially reading a block of data stored consecutively in the memory (column 4, lines 34-53).

26. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device as shown in Hashimoto et al by using address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder for organizing the display data in the memory in an intuitive manner, as shown in Badger, and using the common way of sequentially reading a block of data stored consecutively in the memory as shown in Bloxham et al.

27. Claim 10 is rejected based on the same reason as to claim 5 since they are the software implementation which is necessary to make the circuit in claim 5 operational.

28. Regarding claims 11-13, Badger discloses operating the driving circuit in the first mode includes: setting the line counter to zero; generating consecutive pixel addresses for video data that corresponds to the line counter of zero; and successively increasing the line counter by one and generating corresponding pixel addresses until the last line pointer of the block of line pointers is read out (column 8, lines 16-33, setting initial Y-

Counter, transferring pixel data which would require generating pixel address, and incrementing Y-Counters).

29. Regarding claims 14-15, Badger discloses wherein operating the driving circuit in the first mode includes: setting the line counter to zero; generating consecutive pixel addresses for video data that corresponds to the line counter of zero; transferring the video data with the generated consecutive pixel addresses to the display; and successively increasing the line counter by one, generating corresponding pixel addresses, and transferring video data with the generated corresponding pixel addresses to the display until the last line pointer of the block of line pointers is read out (column 8, lines 16-33, setting initial Y-Counter, transferring pixel data which would require generating pixel address, incrementing Y-Counters, and consecutively transferring pixel data.)

30. Regarding claims 16-18, Badger discloses moving the block of line pointers in the address table register means into the memory (interpreted as saving the line pointers. The operation in Badger, e.g., column 8, lines 16-33, requires saving line pointers, at least temporarily.)

31. Regarding claims 19-21, Bloxham et al, in combination with Hashimoto et al and Badger for video data and display (i.e., pixel data), discloses downloading a first block of line pointers from the memory into the address table register means; transferring video data that corresponds to the first block of the line pointers to the display; and successively downloading next blocks of line pointers from the memory into the address table register means and transferring corresponding video data to the display until the

last block of line pointers of the full table stored in the memory is downloaded from the memory into the address table register means (column 4, lines 55-65, and Fig. 3, data transfer in blocks.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIZE MA whose telephone number is (571)270-3709. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao M. Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628